ABSTRACT OF THE DISCLOSURE

First and second MOS transistors are formed in first and second active areas, respectively, and their gates are configured from a first gate electrode in the first and second transistors. Third and fourth MOS transistors are formed in the second and a third active areas, respectively, and their gates are configured from second and third gate electrodes in the third and fourth transistors. Fifth and sixth MOS transistors are formed in a fourth active area, and their gates are configured from the third and fourth gate electrodes in the fifth and sixth transistors. An end portion of the first gate electrode projecting from the first active area is obliquely arranged relative to a gate width direction of the first transistor, and an end portion of the third gate electrode projecting from the third active area is obliquely arranged relative to a gate width direction of the fourth transistor.